Patent Application No.: 09/874,879
Examiner: Anand S. Rao

Attorney Docket: 2001-0161B
Inventor: Atul Puri

REMARKS

Reconsideration and allowance are requested. Claims 1 - 15 are pending. No claims are amended.

Rejection of Claims 1 - 15 Under Section 102

The Examiner rejects claims 1 - 15 under Section 102 in view of U.S. Patent No. 6,516,090 to Lennon et al. ("Lennon et al."). Applicant respectfully traverses this rejection and submits that Lennon et al. do not anticipate the claims.

Claim 1 recites an apparatus for decoding a bitstream encoded via a plurality of encoders, the bitstream being divided into portions and each portion having an associated model chosen from a plurality of predefined models. The apparatus includes a plurality of decoders and an input switch to route each portion of the bitstream to a decoder based on the associated model of the portion. Applicant respectfully submits that Lennon et al. fail to teach a plurality of decoders as is recited in claim 1.

Lennon et al. disclose a system for video interpretation. They seek to provide a digital image interpretation system wherein the system can automatically identify objects within an image. For example, a vehicle or a person within an image can be identified automatically. What we shall see is that the disclosure of Lennon et al. is not broad enough to encompass a plurality of decoders.

Notably, the Examiner equates column 13, lines 55 - 65 as teaching an apparatus comprising a plurality of decoders. This portion of Lennon et al., however, deals with the *encoding* process. They state:

> In the video segment analyser 140 depicted in FIG. 11, the semantic labels are preferably integrated with the coded digital video signal. If the video segment analyser is integrated with the digital video coding system, the regions may be separately coded in a resolution independent manner. This enables simple reconstruction of a digital video signal at any desired resolution. The method of encoding the digital video signal may be carried out using any of a number of such techniques well known to those skilled in the art.

The on mention of "reconstruction" does not teach or suggest any architecture for such a process. Here they are discussing the video segment analyser 140 of FIG. 11. This device may be part of a digital video coding system or may be separate from such a system. The references in this portion of Lennon et al. are all to the *encoding* process wherein regions within a video image may be separately encoded according to resolution. An example of this may be that a region of a moving vehicle of high interest will be encoded with a higher resolution than a background region that does not move and is of lower interest.

In this regard, Applicant notes that Lennon et al. explain that the video segment analyzer 140 is taught as being integrated with the coding system where a video segment is generated by a segmenter (feature 120 of FIG. 1), and then loaded into the video segment analyzer 140. After all available information is used to analyze the video segment, a labeled RAG (Region Adjacency Graph) is created and transmitted to region encoder that encodes the regions. Col. 13, lines 26 - 40. Therefore, it is clear from this portion of Lennon et al. that they teach a video segment analyzer that performs a *preprocessing* step to the encoding step. In contrast, the present invention is to an apparatus for decoding a bitstream.

The Examiner also cites col. 13, lines 50 - 55 and col. 9, line 20 - 27 as teaching the input switch that routes each portion of the bitstream to a decoder of the plurality of decoders. As discussed above, col. 13, lines 50 - 55 teach a method of *encoding* wherein motion parameters are encoded in block 266 of FIG. 11 and if no motion is detected, then the frame is analysed by a frame event analyzer and the new RAG is generated and encoded by the region encoder 254. Lennon et al.'s disclosure is simply related to the encoding process and not the decoding apparatus of claim 1.

Similarly, col. 9, lines 20 - 27 (as well as lines 3 - 19) teach a frame segmenter 450 that segments the frame into regions and analyses for contextual information and motion vectors. All of this disclosure is related to analyzing the video frame in preparation for encoding the frame. There is simply no mention of a decoding process or an architecture for

decoding as is recited in claim 1. Applicant respectfully submits that because Lennon et al. only teach processing on the encoder side, that Lennon et al. cannot anticipate claim 1. Therefore, claim 1 is patentable and in condition for allowance.

Regarding claims 2 and 3, the Examiner concludes that column 9, lines 20 - 27 anticipates the feature of each decoder being associated with a different predetermined model. This portion of Lennon et al. described the probabilistic-model-based region analyzer 470 that labels the regions in the RAG using an application domain. The result of that process is a labeled RAG that can be used for high-level processes. In sum, this portion of Lennon et al. teaches regarding how to generate a labeled RAG and has nothing to do with the decoding process.

Next, we address what Lennon et al. teach regarding how to process and use the labeled RAG. In col. 13, lines 26 - 37, Lennon et al. state that frame event analyzer 252 receives a video frame and contextual information and produces the labeled RAG. The labeled RAG is output by the frame event analyzer 252 to a region encoder 254 which *then* encodes the RAG. Therefore, the portion of Lennon et al. that the Examiner equates with a decoder being associated with a different predetermined model in fact relates to a pre-processing step that occurs before the encoding process.

Applicant respectfully submits that claims 2 and 3 are not anticipate by Lennon et al. and are in condition for allowance.

The Examiner equates 4 - 5 with the Lennon et al. disclosure in column 12, lines 1 - 41 arguing that they disclose routing a portion to a generic decoder. This portion of Lennon et al. discloses the use of "cliques" in the analysis of regions in the RAG. FIG. 8 lists some cliques for various regions. As such, they provide an aspect of the analysis that is part of the frame event analyzer 202 of FIG. 2. The generation of a labeled RAG is a process that occurs before the encoding process. Therefore, the disclosure regarding "cliques" in column 12 does not teach about a decoding apparatus wherein if a portion of the bitstream cannot be

associated with one of a plurality of predetermined models, the portion is routed to a generic decoder. Further, this portion of Lennon et al. dealing with "cliques" does not teach an output switch for controlling an output signal routed from one of the plurality of decoders.

For these reasons, Applicant submits that claims 4 and 5 are patentable over the prior art of reference.

The remaining claims 6 - 15 each recite similar limitations to at least one limitation discussed above. Each of these claims 6 - 15 recite an apparatus for decoding, which has been addressed above in that Lennon et al. only teach encoding processes and principles. Therefore, each of these claims recites subject matter that is patentable over Lennon et al.

CONCLUSION

Having addressed the rejection of claims 1 - 15, Applicant respectfully submits that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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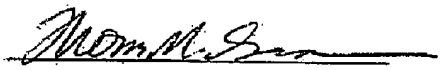
By: 

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